Tunable, Source-Controlled Formation of Platinum Silicides and Nanogaps from Thin Precursor Films

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Controlling the stoichiometry and properties of thin films formed from solid-state reactions is relatively unexplored, yet important for a broad range of applications including many throughout the semiconductor industry.[1,2] Here we use source-limited solid-state diffusion to tune the stoichiometry and properties of thin films of platinum silicide (Pt_xSi), a material with multiple attractive properties for electro-mechanical applications.[3,4] We demonstrate for the first time the formation of Pt_xSi from thin sequentially-deposited layers of platinum (Pt) and amorphous silicon (*a*-Si), and show that the resulting stoichiometry can be tuned over a wide range by simply changing the thickness ratio of the precursor films. Pt-rich silicide films are especially attractive as a contact material for nanoelectromechanical (NEM) contact switches due to the combination of high hardness and elastic modulus, surface stability, and metal-like electrical conductivity. This method of tuning the stoichiometry and properties of thin films is applicable to any metal silicide.

Metal silicides possess a rare combination of thermal stability, mechanical robustness, and metal-like electrical conductivity. This renders them popular in both bulk and thin film form for many structural and electronic applications, such as materials for jet engines, thermoelectric devices, Ohmic and rectifying contacts to silicon, local interconnects, and diffusion barriers.[5] A more recent application involves their use in NEM contact switches. NEM switches are a potential next-generation, low power alternative to fully-electronic complementary metal-oxide semiconductor (CMOS) transistors (**Figure 1**a) that may significantly decrease microprocessor power consumption.[1,2,6] These devices promise orders of magnitude lower power consumption and superior ON/OFF ratios than CMOS (Figure 1b) – a consequence of NEM device topology and the presence of a physical gap between the source and drain terminals.[1,2] NEM switches have also demonstrated applications not accessible with CMOS – most notably exposure to high temperature,[7] radiation,[8,9] and external electric fields.[10] These advantages also render them of interest for future memory technologies.[1] However, the reliability of the contact interface is a concern due to tribological issues, and remains a key challenge for their commercialization.[1,2]

Reliability concerns for NEM contact switches arise from two primary failure mechanisms that are commonly observed in microscale switches:[11–19] device stiction, and contamination/tribopolymer formation. Device stiction, which occurs when the adhesive force between the switch contacts exceeds the restoring force available to open the contact, has been observed for soft,[12] low melting point, highly adhesive, and/or miscible[11,13] contact interfaces such as Au/Au or Au/Pt.[11,12,14] The adhesive interactions often increase over the switch lifetime due to surface deformations that increase contact areas.[15] Therefore, contact materials should have a high hardness and elastic moduli. Contamination/tribopolymer formation, which increases the contact resistance with continued cycling, results from mechanochemically-induced growth of insulating material at contact interfaces.[16,17] Tribopolymer formation has been observed even for unreactive noble metal contacts such as Pt, Ru, and Ir[18–20] and has been correlated with the cleanliness of the environment surrounding the contact.[16] In an early comprehensive study of tribopolymer formation, Hermance and Egan found that hydrocarbon concentrations of 5 ppm were sufficient for insulating tribopolymer buildup on macroscopic precious metal contacts.[21] These failure mechanisms are exacerbated in NEM switches, where low contact and restoring forces required for reliable operation (10^{16} contact cycles are desirable[1]) may be insufficient to penetrate adsorbed films or to separate adhesive contacts. Thus, both stiction and tribopolymer formation constitute the main challenges for NEM switch commercialization and call for developing new materials with reliably low contact resistance, low adhesion, high hardness and elastic modulus, and resistance to tribofilm formation.[20]

Platinum silicide (Pt_xSi) possesses several appealing characteristics that make it an attractive switch contact material candidate. Pt_xSi was first investigated in the 1980s as an electrical contact material with high conductivity in fully-electronic, Si-based devices.[3] More recently, Pt_xSi films have demonstrated wear and oxidation resistance during nanoscale mechanical contact.[4] Conversion of Pt and single-crystal silicon (*sc*-Si) to Pt_xSi results in approximately 15% volumetric shrinkage[3] and may be exploited to separate buried material interfaces. Pt_xSi could therefore be used to release NEM switches with a self-formed gap caused by interfacial separation driven by

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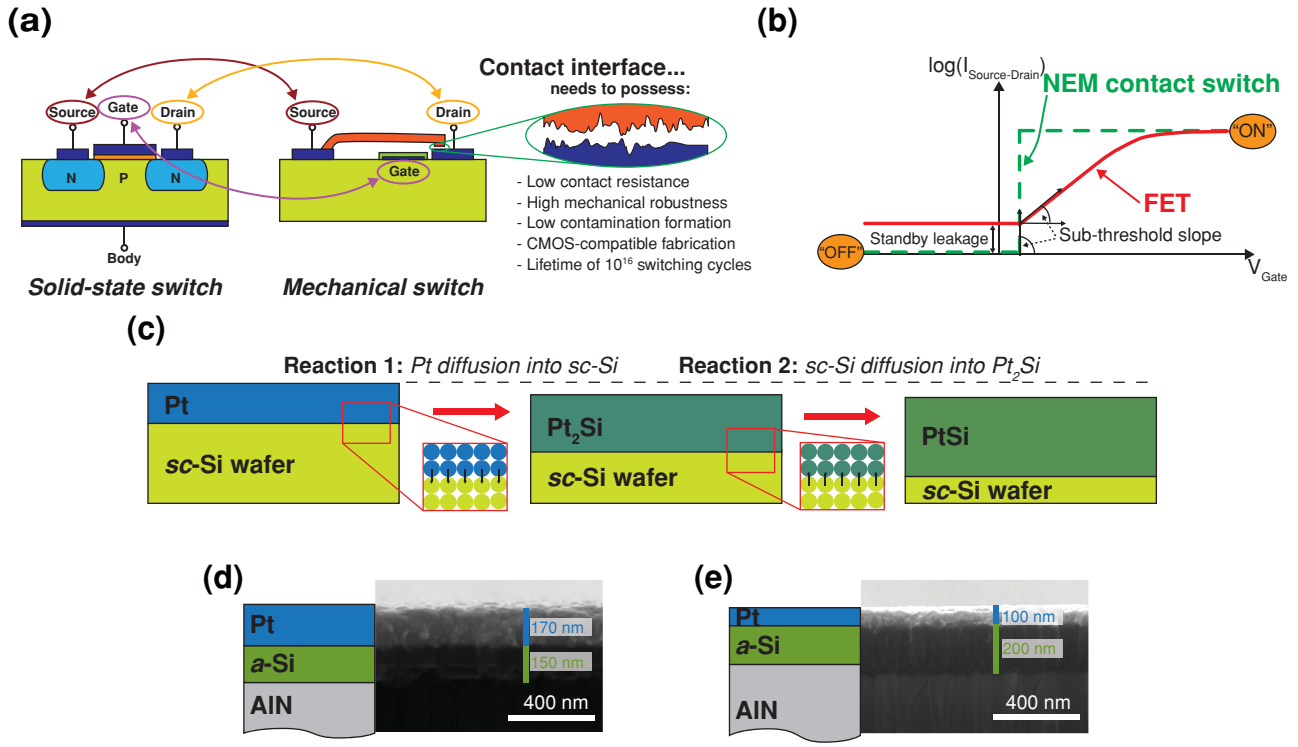

Figure 1. Structural and performance comparison of a solid-state and a mechanical switch and schematics of *sc*-Si/Pt silicidation and *a*-Si/Pt samples. a, Schematic of a typical solid-state switch and an electrostatically actuated mechanical switch that highlights the structural analogies between both switch types. The magnified view to the right illustrates the physical separation between source and drain in the mechanical switch in its OFF state and emphasizes the demanding requirements on contact materials in nanoscale mechanical switches, which are a consequence of the harsh operating conditions (high contact stresses and current densities). b, Schematic current-voltage plots comparing the performance of a NEM contact switch with that of a field-effect transistor (FET), taken as an example of solid-state switches. The gate voltage (V_{Gate}) is increased to turn the switch on, resulting in current flow between source and drain. The higher subthreshold slope of NEM switches allows for lower gate voltages; combined with far lower standby leakage, this greatly reduces device power consumption. c, Schematic of typical Pt_xSi formation using a thin layer of Pt deposited onto a cleaned *sc*-Si wafer, and subsequently annealed. In the first reaction, the Pt diffuses into the *sc*-Si and the intermediate Pt-rich silicide Pt_2Si is formed. After all Pt is consumed, the *sc*-Si diffuses into Pt_2Si to form the thermodynamically stable PtSi phase. The temperature range of the Pt_2Si formation (180–200 °C) and the PtSi formation (280–400 °C) are within the thermal budged of most CMOS processes. d, Schematic and SEM cross-section image of the as-deposited Pt:*a*-Si = 1:1 sample. e, Schematic and SEM cross-section image of the as-deposited Pt:*a*-Si = 1:2 sample.

shrinkage-induced tensile stress. Nguyen *et al.* recently demonstrated the release of free-standing MEMS structures with Ti/Si and Mo/Si chemistries,[22] a task traditionally accomplished using costly and time-consuming sacrificial Si release etches. Silicide-based release of buried interfaces would also eliminate exposure to air, preventing adsorption of carbon, oxygen, and other contaminants which profoundly affect device operation.

Pt_xSi formed from thin film Pt and a *sc*-Si wafer is described by a two-reaction process (Figure 1c).[23,24] Since common NEM switch geometries[2,25] demand silicidation away from the *sc*-Si carrier wafer, the *sc*-Si/Pt silicidation process is incompatible with NEM switch geometries, especially if co-integration with CMOS is desired. Furthermore, silicide-release using existing device topologies would require silicidation on both the top and bottom of features, which is not compatible with *sc*-Si/Pt process. Instead, Pt_xSi must be formed from precursors both deposited as thin films, necessitating the use of either polycrystalline Si or amorphous silicon (*a*-Si) precursor films; *a*-Si's homogeneity renders it preferable.

Little is known about the Pt_xSi formation using an *a*-Si precursor. Ito *et al.* investigated Pt_xSi formation with hydrogenated *a*-Si (*a*-Si:H) and found the simultaneous existence of PtSi, Pt_2Si, and incompletely consumed initial Pt.[26] Impurities at the silicidation boundary, mainly hydrogen from the *a*-Si:H film, were hypothesized to limit Pt consumption. Here, thin layers of *a*-Si and Pt are employed instead. We hypothesize that the relative thicknesses of *a*-Si and Pt films control the stoichiometry and resulting mechanical and electrical properties of the silicide product. This methodology differs significantly from the formation of Pt_xSi from a thin Pt layer on a *sc*-Si wafer, which constitutes an unlimited supply of Si.

Samples with two Pt:*a*-Si film thickness ratios – 1:1 and 1:2 – were fabricated to explore the effect of precursor material thickness on silicide stoichiometry (Figure 1d and 1e) and the resulting mechanical and electrical properties. To achieve this, a *sc*-Si carrier wafer was first sputter-coated with aluminium nitride (AlN, thickness: 3 µm) to act as a diffusion barrier between the silicide and carrier wafer. The deposition of AlN also mimics the topology of existing piezoelectrically-actuated NEM switch prototypes.[25] Thin layers of *a*-Si and Pt of 100–200 nm-thickness were subsequently sputter-coated on top of the AlN layer. The *a*-Si and Pt depositions were conducted

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sequentially in the same deposition system with vacuum maintained, thus minimizing adsorbed contamination between the layers and oxidation of the *a*-Si, both of which would inhibit silicidation. The samples were then removed from the deposition system and subsequently annealed for 6 hours at 500 °C inside an X-ray photoelectron spectrometer (XPS) in high vacuum ($<1\cdot10^{-8}$ Torr),[27] while continuously monitoring the Pt 4f and Si 2p XP signals. High-resolution angle-resolved XPS analysis of the near-surface region before and at the end of the annealing process allowed the stoichiometry of the as-deposited Pt and formed Pt_xSi, as well as its in-depth homogeneity, to be determined. Nanoindentation of the as-deposited and annealed samples was used to determine film modulus and hardness. Conductive atomic force microscopy (C-AFM) was performed to evaluate contact resistance and surface morphology of the as-deposited Pt and formed Pt_xSi films. All experiments were repeated twice to ensure reproducibility.

The high-resolution XPS (HR-XPS) Pt 4f spectrum of as-deposited Pt (from the Pt:*a*-Si = 1:1 sample; note: identical spectra were obtained with the Pt:*a*-Si = 1:2 sample) is displayed in **Figure 2**c. The Pt 4f peak consists of two components, Pt $4f_{7/2}$ and Pt $4f_{5/2}$, due to spin-orbit coupling. Both peak position (70.90 eV) and lineshape of the Pt $4f_{7/2}$ are characteristic of metallic platinum. Upon annealing, the Pt $4f_{7/2}$ spectra of both Pt:*a*-Si ratios (i.e., Pt:*a*-Si = 1:1 in Figure 2b and Pt:*a*-Si = 1:2 in Figure 2a) exhibited a multicomponent character: besides metallic platinum (70.90 eV), three new components appeared at 71.47, 72.14, and 72.50 eV, assigned to Pt_3Si, Pt_2Si, and PtSi, respectively. The relative concentrations of Pt, Pt_3Si, Pt_2Si, and PtSi are reported in the insets in Figure 2. The Pt:*a*-Si = 1:1 sample produced a dominant Pt_3Si/Pt_2Si phase mixture (74%), while the Pt:*a*-Si = 1:2 sample produced mostly PtSi (71%) with little Pt_2Si (23%) remaining. This demonstrates that the near-surface stoichiometry of Pt_xSi can be tuned by varying the thickness ratio of Pt and *a*-Si, and that Pt_xSi formation occurs at CMOS compatible temperatures (400–425 °C).

We analyzed the silicide samples using the continuous stiffness measurement (CSM) nanoindentation method[30] and depth-controlled nanoindentation to reveal the changes in hardness and modulus due to silicidation of the two samples. It should be noted that, to characterize the mechanical properties of a thin film, two possible artifacts must be mitigated: (1) a surface roughness effect (at small indentation depths comparable to the surface roughness), inducing an underestimation of the hardness and modulus due to the incompact surface; and (2) a substrate effect (at large indentation depths beyond 20% of the film thickness), inducing an overestimation of the hardness and modulus due to the stiffer, harder AlN substrate. The CSM method, which enables the measurement of the modulus and hardness as a function of indentation depth, was used to

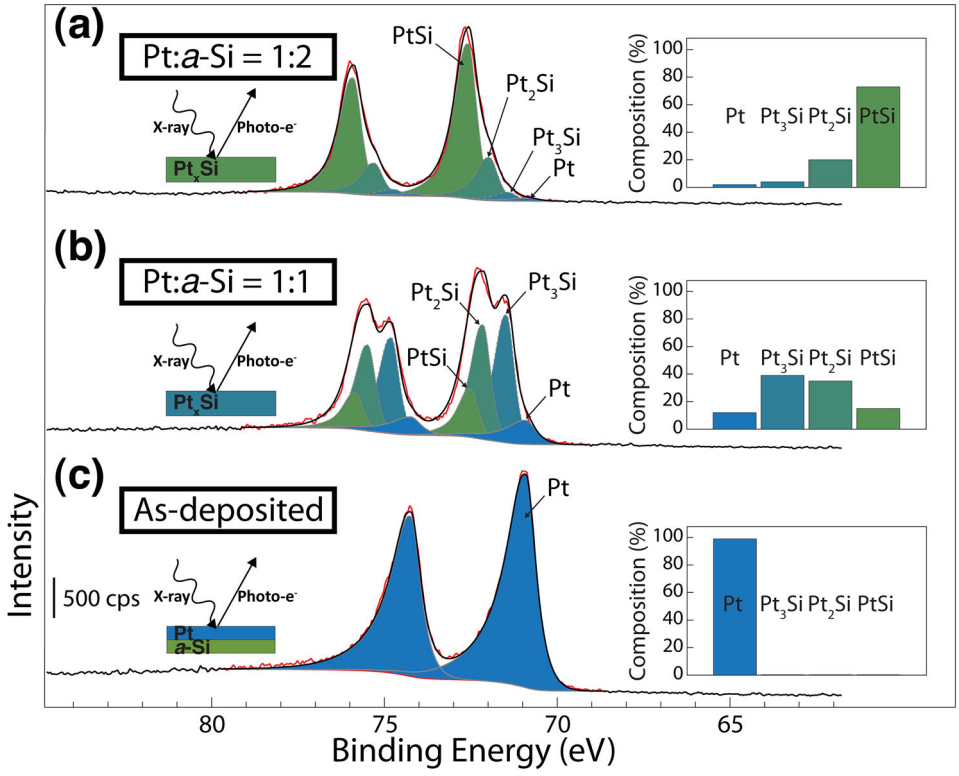

Figure 2. Surface characterization of as-deposited Pt and formed Pt_xSi. a, High-resolution XPS spectra of the Pt 4f peaks of the annealed Pt:*a*-Si = 1:2 spectra. The Pt 4f peaks shift to higher binding energies indicating Pt_xSi formation. The near-surface composition of the annealed Pt:*a*-Si = 1:2 sample is dominated by Si-rich PtSi. b, High-resolution XPS spectra of the Pt 4f peaks of the annealed Pt:*a*-Si = 1:1 spectra. The Pt 4f peaks shift to higher binding energies indicating Pt_xSi formation. Near-surface composition of the annealed Pt:*a*-Si = 1:1 sample dominated by Pt-rich Pt_3Si/Pt_2Si. c, High-resolution XPS spectra of the Pt 4f peaks of the as-deposited sample. The Pt 4f peaks indicate the presence of pure metallic Pt.

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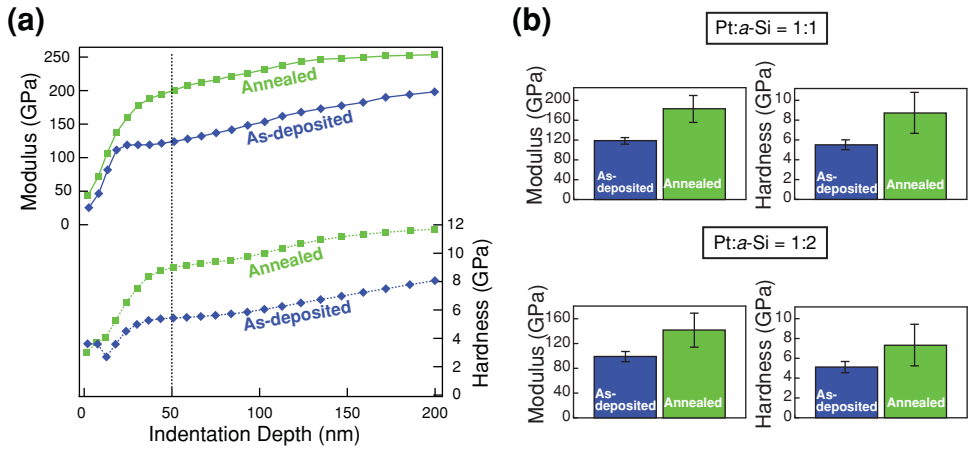

Figure 3. Nanoindentation of as-deposited Pt and formed Pt_xSi. a, Modulus and hardness as a function of indentation depth curves for the Pt:*a*-Si = 1:1 sample in the as-deposited and annealed state. Both modulus and hardness shoulder at approximately 50 nm indentation depth, indicating that this depth is ideal for measuring the thin film properties. b, Average modulus and hardness values and their standard derivations obtained from 100 depth-controlled indentations at 50 nm indentation depth for the Pt:*a*-Si = 1:1 and Pt:*a*-Si = 1:2 samples in their as-deposited and annealed states. For both Pt:*a*-Si ratios, the modulus and hardness significantly increased due to the Pt_xSi formation compared to the as-deposited film.

determine the appropriate range of indentation depths to minimize the two aforementioned effects. **Figure 3**a shows the CSM modulus and hardness curves for the Pt:*a*-Si = 1:1 sample in the as-deposited condition and after annealing. Both the modulus and hardness curves show a shoulder at approximately 50 nm indentation depth, indicating that this depth corresponds to minimized surface roughness and substrate effects. Similar tests on the Pt:*a*-Si = 1:2 sample also found the optimal sampling depth to be 50 nm. Therefore, measurements at this depth are used to extract the mechanical properties of the films. Figure 3b summarizes the modulus and hardness values obtained after performing approximately 100 50-nm indents on the two samples in the as-deposited and annealed states. For both samples, the modulus and hardness increases by approximately 50% due to annealing. Thus, both silicide films are mechanically more robust and will therefore be significantly more resistant to mechanical degradation than the as-deposited Pt films from which they originated. These results represent the first reported values for modulus and hardness measurements on Pt_xSi.

We further analyzed the silicide samples using conductive atomic force microscopy (C-AFM) measurements to determine the contact resistance of the silicide films of different stoichiometries compared to as-deposited Pt. **Figure 4**a–c show contact resistance color relief maps of representative areas of as-deposited Pt, the annealed Pt:*a*-Si = 1:1 sample, and the annealed Pt:*a*-Si = 1:2 sample, respectively. Insets show the distribution of contact resistance values over the probed area; variations are due to grain boundaries, roughness, and contamination. The distribution shifts to higher values with increasing *a*-Si film thickness and thereby with increasing Si-content in the silicide film (see Figure 2). The minimum contact resistance values encountered during the scan are 4.65 kΩ for as-deposited Pt, 5.14 kΩ for the Pt:*a*-Si = 1:1 sample and 9.37 kΩ for the Pt:*a*-Si = 1:2 sample (Figure 4d). The minimum contact resistance of both silicide stoichiometries is less than twice the value measured for as-deposited Pt. This shows that the silicide films possess a metallic-like contact resistance. The minimum contact resistance increase of the Pt-rich silicide film (Pt:*a*-Si = 1:1) compared to as-deposited Pt film is modest (<10%), and well within ranges needed for NEM switch applications. The coupling between contact resistance and *a*-Si content in the silicide film demonstrates that we can control the electronic properties of the silicide by changing the Pt:*a*-Si layer ratio and thereby the silicide stoichiometry.

Finally, we demonstrate nanoscale gap formation using a silicide-based release process with Pt_xSi formed from *a*-Si and Pt for the first time in Figure 4e. The Pt layer diffused into the *a*-Si layers above and below upon rapid thermal annealing (5 minutes, 600 °C, in nitrogen), to form two Pt_xSi layers cleanly separated by a 10–15 nm gap, a geometry that is rather involved to form using sacrificial etch processes. This vacuum gap is protected from air exposure which can be desirable for NEM applications where avoiding contamination is critical.

In summary, we present a novel technique for forming Pt_xSi thin films from solid thin film precursors. The stoichiometry and its mechanical and electrical properties can be controllably pre-determined by changing the Pt:*a*-Si layer thickness ratio from which the silicide films originate. We further demonstrate, for the first time, the viability of Pt_xSi films for NEM switch applications. The Pt-rich silicide films possess a modest increase in contact resistance compared to as-deposited Pt, and exhibit a 50% increase in modulus and hardness. We propose that these films may be ideal materials for NEM contact switches and may ultimately enable the commercialization of these devices. Additionally, we predict that our method of adjusting the silicide stoichiometry and properties by changing the precursor layer thickness ratios will be also applicable to other metal silicides (e.g., titanium, nickel, tungsten, cobalt, molybdenum, and chromium silicide).

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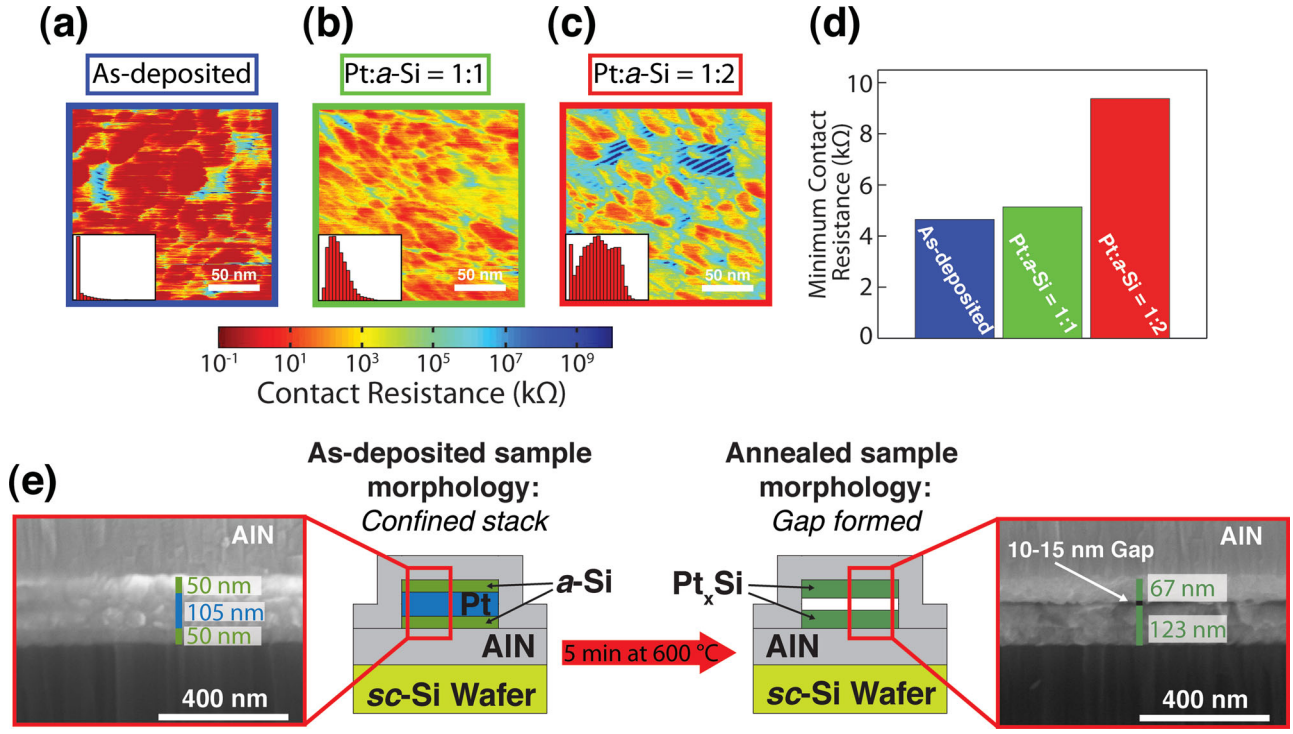

Figure 4. Conductive atomic force microscopy measurements of as-deposited Pt and annealed Pt_xSi samples and schematic of Pt_xSi-based silicide release. a-c, Contact resistance color relief maps of a representative 200 nm × 200 nm scan on a representative a) as-deposited Pt film, b) annealed Pt:*a*-Si = 1:1, and c) annealed Pt:*a*-Si = 1:2. Insets show the contact resistance distribution obtained from each scan. The contact resistance distribution shifts towards higher contact resistances with increasing *a*-Si availability from a-c. d, Minimum contact resistance values encountered during the 200 nm x 200 nm scans. Annealed Pt:*a*-Si = 1:1 film possesses contact resistance values approximately 10% higher than those seen in pure Pt films. The higher *a*-Si content in the Pt:*a*-Si = 1:2 film leads to a further increased contact resistance to approximately twice the value of as-deposited Pt. However, these values are still within the same order of magnitude of pure Pt and well within acceptable bounds for NEM switches. e, Schematic and SEM cross-section of the Pt_xSi-based silicide-release process. A Pt layer, which is initially sandwiched between two *a*-Si layers, diffuses into the *a*-Si layers upon rapid thermal annealing for 5 minutes at 600 °C and two completely separated Pt_xSi layers are formed.

Experimental Section

Film Deposition: The Pt and *a*-Si films were sputter deposited in a Denton Vacuum Explorer 14 sputterer (Denton Vacuum Inc, Moorestown, NJ, USA) with a purity of 99.99% for both films. Pt was deposited in DC mode at 450 W and *a*-Si in AC mode at 230 W. All samples were produced in duplicate and the experiments were repeated to ensure reproducibility.

Annealing: The annealing of the Pt/*a*-Si films to form Pt_xSi was performed inside a customized XPS spectrometer (VG Scienta AB, Uppsala, Sweden).[27] The samples (6×6 mm^2) were mounted in a holder (RHK Technology Inc., Troy, MI, USA) that included a tungsten filament for radiative heating. The temperature was measured using a K-type thermocouple in contact with the sample. The films were annealed in progressive steps from 25 °C to 500 °C at 25 °C intervals with 12 minute holding times at each interval to perform XPS measurements. After reaching 500 °C, the films were annealed for 6 hours and then cooled down to room temperature (cooling rate: 10 °C·min^{-1}).

In situ/ex situ XPS Analysis: The chemistry of the near-surface region was investigated by XPS using a customized XPS spectrometer (VG Scienta AB, Uppsala, Sweden).[27] XPS analyses were performed using a monochromatic Al Kα source (photon energy: 1486.6 eV). The residual pressure in the analysis chamber was constantly less than $1 \cdot 10^{-8}$ Torr. The spectrometer was calibrated according to ISO 15472:2001 with an accuracy of ± 0.05 eV. Survey and high-resolution spectra were acquired in constant-analyzer-energy mode with the pass energies of 200 eV and 100 eV, respectively. The full width at half-maximum (FWHM) of the peak-height for the high-resolution $Ag_{3d5/2}$ signal of a sputter-cleaned Ag sample was 0.57 eV. The spectra were processed using CasaXPS software (v.2.3.16, Case Software Ltd., Wilmslow, Cheshire, U.K.). Background subtraction was performed using the Shirley-Sherwood method. The quantitative evaluation of XPS data was based on integrated intensity using a first-principles model and applying Powell's equation.[28] The inelastic mean free path was calculated using the TPP-2M formula.[29] Curve synthesis for the Pt 4f peaks was performed constraining the integrated intensity ratio of these two signals to 3:4 and their energy separation to 3.33 eV. The reference energies for Pt $4f_{7/2}$ peaks are 70.90 eV, 71.47 eV, 72.14 eV, and 72.50 eV for Pt, Pt_3Si, Pt_2Si, and PtSi respectively.

Nanoindentation: The mechanical properties of the thin films were evaluated using an Agilent™ Nano Indenter G200 (Agilent Technologies, Santa Clara, CA) in the continuous stiffness measurement (CSM) method[30] and a Hysitron TI 950 TriboIndenter (Hysitron Corp., Minneapolis, MN) in depth-controlled indentation mode. Twenty CSM indents and 100 depth-controlled indents per sample were performed. In both cases, a Berkovich diamond tip was used.

Conductive Atomic Force Microscopy: C-AFM scans (200 nm × 200 nm scan size) were performed in an Asylum MFP-3D (Asylum Research, Santa Barbara, CA) in dry nitrogen environment (RH < 3%). An AFM probe with 70 nm Pt sputter-coated on the tip (Nanosensors PPP-CONT, Nanosensors, Neuchatel, Switzerland) was used with a 15 nN contact force and a 100 mV bias voltage. A home-built logarithmic current amplifier was used. To account for the presence of noise and variability in the current measurements due to contamination and

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inhomogeneities, we used the average of the upper 5% of the current distribution measured during the C-AFM scan to calculate the minimum contact resistance (Figure 4d).

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